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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,474	08/27/2003	Arkadiy Morgenshtein	26327	5738

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EXAMINER

CHANG, DANIEL D

ART UNIT	PAPER NUMBER
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2819

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/648,474

Applicant(s)

MORGENSHTEIN ET AL.

Examiner

Daniel D. Chang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 June 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-54 is/are pending in the application.
4a) Of the above claim(s) 47-54 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-3, 5-18, 20-35, 37-46 is/are rejected.
7) ☒ Claim(s) 4, 19 and 36 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Acknowledgement

Receipt is acknowledged of the Amendment filed June 1, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-18, 20-35, and 37-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Daniele et al. (US 5,412,599, hereinafter Daniele).

Regarding claim 1, Daniele discloses, at least in figures 8, 17, and 18, a complementary logic circuit, comprising:

- a first logic input (gate of T1; 28);

- a second logic input (gate of T2; 30);

- a first dedicated logic terminal (IN2);

- a second dedicated logic terminal (IN1);

- a first logic block (see 12, 30 in Fig. 8) comprising:

- a p-type transistor network (T2) for implementing a predetermined logic function, said network having an outer diffusion connection (top portion of T2 in Fig. 8), a first network gate connection (30), and an inner diffusion connection (12), said outer diffusion connection of said p-type transistor network being connected to said first dedicated logic terminal (IN2), and said first network gate connection of said p-type transistor network being connected to said first logic input (30); and

- a second logic block (see 24, 28 in Fig. 8) comprising:

- an n-type transistor network (T1) implementing logic function complementary to said

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predetermined logic function, said network having an outer diffusion connection (24 in Fig. 8), a first network gate connection (28), and an inner diffusion connection (top portion of T1 in Fig. 8),

said outer diffusion connection of said n-type transistor network being connected to said second dedicated logic terminal (IN 1), and said first network gate connection of said n-type transistor network being connected to said second logic input (28);

said inner diffusion connections of said p-type transistor network (12) and of said n-type transistor network (top portion of T1 in Fig. 8) being connected to form a common diffusion logic terminal.

Regarding claim 2, Daniele discloses, at least in figures 8, 17, and 18, that the first and second logic inputs are connected to form a first common logic input (42).

Regarding claim 3, Daniele discloses, at least in figures 8, 17, and 18, that each of said logic terminals is separately configurable to serve as a logic input (IN1, IN2).

Regarding claim 5, Daniele discloses, at least in figures 8, 17, and 18, a third logic input connected to a second network gate connection of said p-type transistor network (see col. 11, line 43 - col. 12, line 31).

Regarding claim 6, Daniele discloses, at least in figures 8, 17, and 18, a fourth logic input connected to a second network gate connection of said n-type transistor network (see col. 11, line 43 - col. 12, line 31).

Regarding claim 7, Daniele discloses, at least in figures 8, 17, and 18, a fourth logic input connected to a second network gate connection of said n-type transistor network (see col. 11, line 43 - col. 12, line 31).

Regarding claim 8, Daniele discloses, at least in figures 8, 17, and 18, that said third and fourth logic inputs being connected to form a second common logic input (see col. 11, line 43 - col. 12, line 31).

Regarding claim 9, Daniele discloses, at least in figures 8, 17, and 18, that said p-type transistor network comprises a single p-type transistor (T2).

Regarding claim 10, Daniele discloses, at least in figures 8, 17, and 18, said n-type transistor network comprises a single n-type transistor (T1).

Regarding claim 11, Daniele discloses, at least in figures 8, 17, and 18, that said p-type transistor network comprises one of a group of networks comprising: a network of p-type field effect transistors (FET), a network of p-type p-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type n-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type twin-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type silicon on insulator (SOI) transistors, and a network of p-type silicon on sapphire (SOS) transistors (col. 6, lines 10+).

Regarding claim 12, Daniele discloses, at least in figures 8, 17, and 18, that said n-type transistor network comprises one of a group of networks comprising: a network of n-type FETs, a network of n-type p-well CMOS transistors, a network of n-type n-well CMOS transistors, a network of n-type twin-well CMOS transistors, a network of n-type SOI transistors, and a network of n-type SOS transistors (col. 6, lines 10+).

Regarding claim 13, Daniele discloses, at least in figures 8, 17, and 18, that one of a group of logic circuits comprising: an OR gate, an inverted OR (NOR) gate, an AND gate, a multiplexer gate, an inverter gate, and an exclusive OR (XOR) gate (col. 6, lines 10+).

Regarding claim 14, Daniele discloses, at least in figures 8, 17, and 18, that said logic circuit is operable to implement a ((NOT A) OR B) logic operation upon logic inputs A and B (Fig. 25, col. 12, lines 29+).

Regarding claim 15, Daniele discloses, at least in figures 8, 17, and 18, that said logic circuit is operable to implement a ((NOT A) AND B) logic operation upon logic inputs A and B (Fig. 25,

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col. 12, lines 29+).

Claims 16-18, 20-24, and 26 are essentially the same in scope as claims discussed above and are rejected similarly.

Regarding claims 25 and 27-32, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Claims 33-35 and 37-46 are essentially the same in scope as claims discussed above and are rejected similarly.

Response to Arguments

Applicant's arguments with respect to claims 1-46 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claims 4, 19, and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

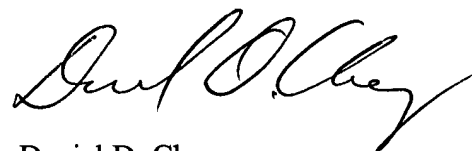
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER